Thyristor/Diode and Thyristor/Thyristor (ADD-A-PAK^{TM} Generation 5 Power Modules), 75/95 A

ADD-A-PAK^{TM}

PRODUCT SUMMARY	
$I_{T(AV)}$ or $I_{F(AV)}$	75/95 A

MECHANICAL DESCRIPTION

The Generation 5 of ADD-A-PAK^{TM} modules combine the excellent thermal performance obtained by the usage of Direct Bonded Copper substrate with superior mechanical ruggedness, thanks to the insertion of a solid copper baseplate at the bottom side of the device. The Cu baseplate allows an easier mounting on the majority of heatsink with increased tolerance of surface roughness and improved thermal spread. The Generation 5 of AAP modules is manufactured without hard mold, eliminating in this way any possible direct stress on the leads.
The electrical terminals are secured against axial pull-out: they are fixed to the module housing via a click-stop feature already tested and proved as reliable on other Vishay HPP modules.

FEATURES

- High voltage
- Industrial standard package
- Thick copper baseplate
- UL E78996 approved
- 3500 V_{RMS} isolating voltage
- Totally lead (Pb)-free
- Designed and qualified for industrial level

Pb-free
RoHS COMPLIANT

BENEFITS

- Up to 1600 V
- Fully compatible TO-240AA
- High surge capability
- Easy mounting on heatsink
- Al_20_3 DBC insulator
- Heatsink grounded

ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

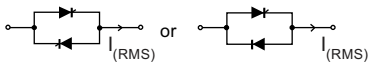
MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS	VSK.71	VSK.91	UNITS
$I_{T(AV)}$ or $I_{F(AV)}$	85 °C	75	95	A
$I_{O(RMS)}$	As AC switch	165	210	
I_{TSM}, I_{FSM}	50 Hz	1665	1785	
	60 Hz	1740	1870	
I^2t	50 Hz	13.86	15.91	kA^2s
	60 Hz	12.56	14.52	
$I^2\sqrt{t}$		138.6	159.1	$kA^2\sqrt{s}$
V_{RRM}	Range	400 to 1600		V
T_{Stg}		- 40 to 125		°C
T_J				

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V_{DRM}, MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I_{RRM}, I_{DRM} AT 125 °C mA
VSK.71/.91	04	400	500	400	15
	06	600	700	600	
	08	800	900	800	
	10	1000	1100	1000	
	12	1200	1300	1200	
	14	1400	1500	1400	
	16	1600	1700	1600	

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VSK.71	VSK.91	UNITS
Maximum average on-state current (thyristors)	$I_{T(AV)}$	180° conduction, half sine wave, T_C = 85 °C			75	95	A
Maximum average forward current (diodes)	$I_{F(AV)}$						
Maximum continuous RMS on-state current, as AC switch	$I_{O(RMS)}$				165	210	
Maximum peak, one-cycle non-repetitive on-state or forward current	I_{TSM} or I_{FSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T_J = T_J maximum	1665	1785	
		t = 8.3 ms			1740	1870	
		t = 10 ms	100 % V_{RRM} reapplied		1400	1500	
		t = 8.3 ms			1470	1570	
		t = 10 ms	T_J = 25 °C no voltage reapplied		1850	2000	
		t = 8.3 ms			1940	2100	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied	Initial T_J = T_J maximum	13.86	15.91	kA^2s
		t = 8.3 ms			12.56	14.52	
		t = 10 ms	100 % V_{RRM} reapplied		9.80	11.25	
		t = 8.3 ms			8.96	10.27	
		t = 10 ms	T_J = 25 °C, no voltage reapplied		17.11	20.00	
		t = 8.3 ms			15.60	18.30	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$ (1)	t = 0.1 to 10 ms, no voltage reapplied T_J = T_J maximum			138.6	159.1	$kA^2\sqrt{s}$
Maximum value or threshold voltage	$V_{T(TO)}$ (2)	Low level (3)	T_J = T_J maximum		0.82	0.80	V
		High level (4)			0.85	0.85	
Maximum value of on-state slope resistance	r_t (2)	Low level (3)	T_J = T_J maximum		3.00	2.40	mΩ
		High level (4)			2.90	2.25	
Maximum peak on-state or forward voltage	V_{TM}	$I_{TM} = \pi \times I_{T(AV)}$	T_J = 25 °C		1.59	1.58	V
	V_{FM}	$I_{FM} = \pi \times I_{F(AV)}$					
Maximum non-repetitive rate of rise of turned on current	dI/dt	T_J = 25 °C, from 0.67 V_{DRM}, $I_{TM} = \pi \times I_{T(AV)}$, I_g = 500 mA, t_r < 0.5 µs, t_p > 6 µs			150		A/µs
Maximum holding current	I_H	T_J = 25 °C, anode supply = 6 V, resistive load, gate open circuit			250		mA
Maximum latching current	I_L	T_J = 25 °C, anode supply = 6 V, resistive load			400		

Notes

(1) I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$

(2) Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$

(3) 16.7 % x π x I_{AV} < I < π x I_{AV}

(4) I > π x I_{AV}

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VSK.71	VSK.91	UNITS
Maximum peak gate power	P_{GM}			12		W
Maximum average gate power	$P_{G(AV)}$			3.0		
Maximum peak gate current	I_{GM}			3.0		A
Maximum peak negative gate voltage	$-V_{GM}$			10		V
Maximum gate voltage required to trigger	V_{GT}	T_J = - 40 °C	Anode supply = 6 V resistive load	4.0		
		T_J = 25 °C		2.5		
		T_J = 125 °C		1.7		
Maximum gate current required to trigger	I_{GT}	T_J = - 40 °C	Anode supply = 6 V resistive load	270		mA
		T_J = 25 °C		150		
		T_J = 125 °C		80		
Maximum gate voltage that will not trigger	V_{GD}	T_J = 125 °C, rated V_{DRM} applied		0.25		V
Maximum gate current that will not trigger	I_{GD}	T_J = 125 °C, rated V_{DRM} applied		6		mA

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VSK.71	VSK.91	UNITS
Maximum peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	I_{RRM}, I_{DRM}	T_J = 125 °C, gate open circuit	15		mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted	2500 (1 min) 3500 (1 s)		V
Maximum critical rate of rise of off-state voltage	dV/dt (1)	T_J = 125 °C, linear to 0.67 V_{DRM}	500		V/µs

Note

(1) Available with dV/dt = 1000 V/ms, to complete code add S90 i.e. VSKT91/16AS90

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VSK.71	VSK.91	UNITS
Junction operating and storage emperature range	T_J, T_{Stg}		- 40 to 125		°C
Maximum internal thermal resistance, junction to case per module	R_{thJC}	DC operation	0.165	0.135	K/W
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface flat, smooth and greased	0.1		
Mounting torque ± 10 % to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	5		Nm
Mounting torque ± 10 % busbar			3		
Approximate weight			110		g
			4		oz.
Case style		JEDEC	TO-240AA		

ΔR CONDUCTION PER JUNCTION

DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.71	0.06	0.07	0.09	0.12	0.18	0.04	0.08	0.10	0.13	0.18	°C/W
VSK.91	0.04	0.05	0.06	0.08	0.12	0.03	0.05	0.06	0.08	0.12	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

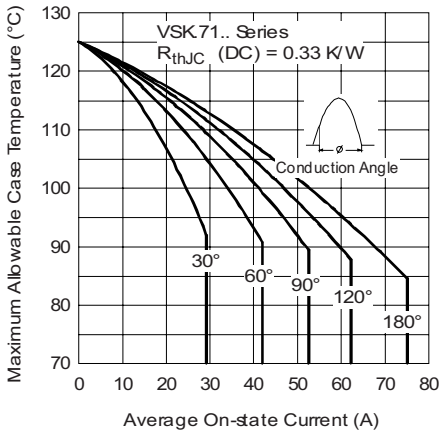


Fig. 1 - Current Ratings Characteristics

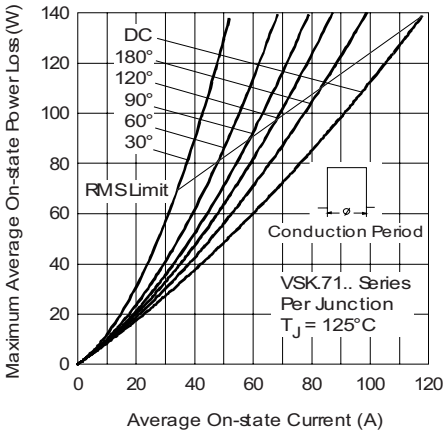


Fig. 4 - On-State Power Loss Characteristics

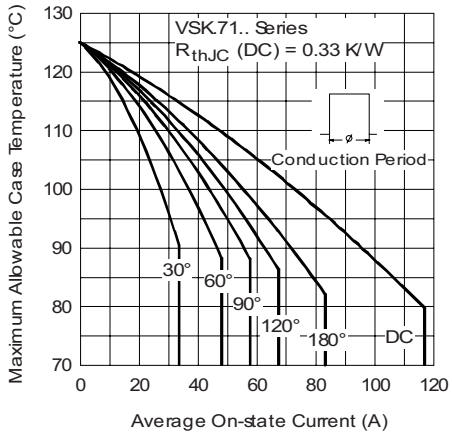


Fig. 2 - Current Ratings Characteristics

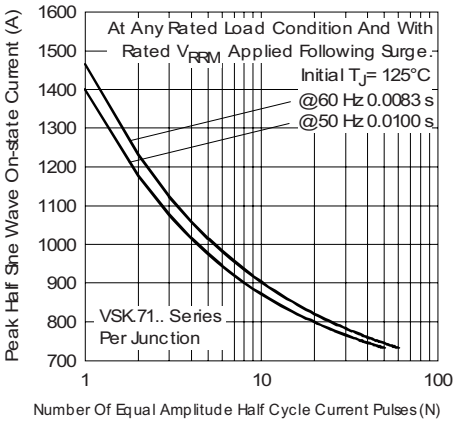


Fig. 5 - Maximum Non-Repetitive Surge Current

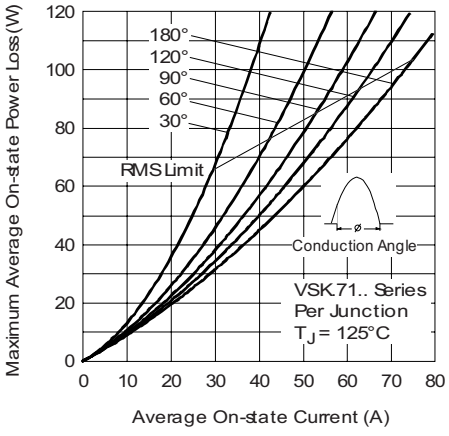


Fig. 3 - On-State Power Loss Characteristics

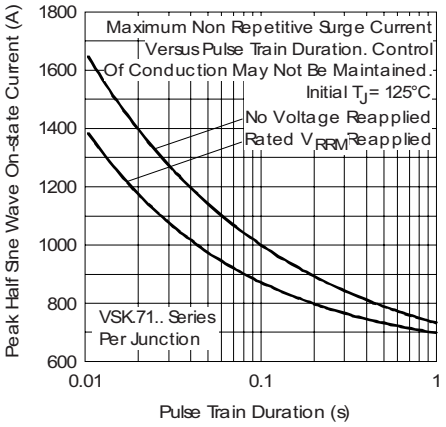


Fig. 6 - Maximum Non-Repetitive Surge Current

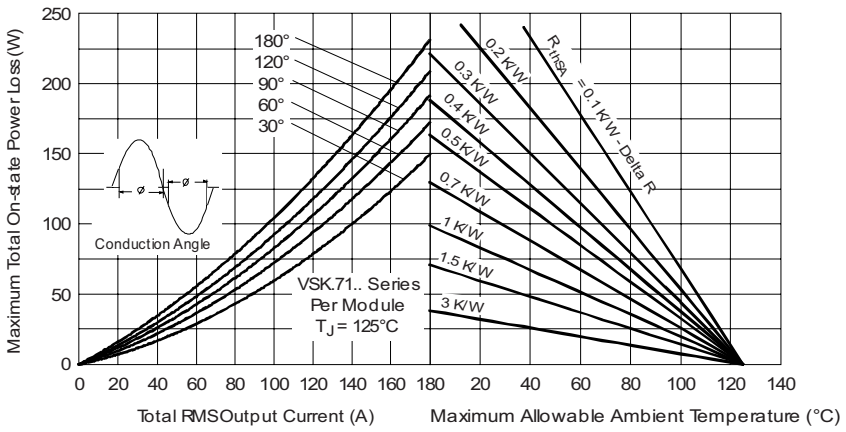


Fig. 7 - On-State Power Loss Characteristics

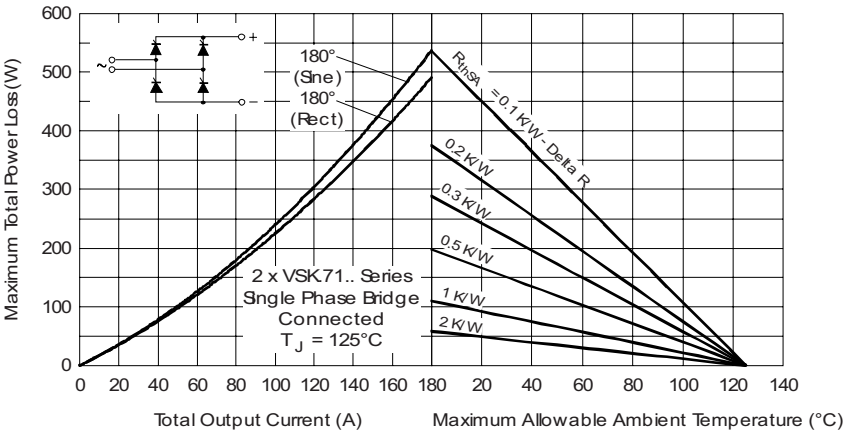


Fig. 8 - On-State Power Loss Characteristics

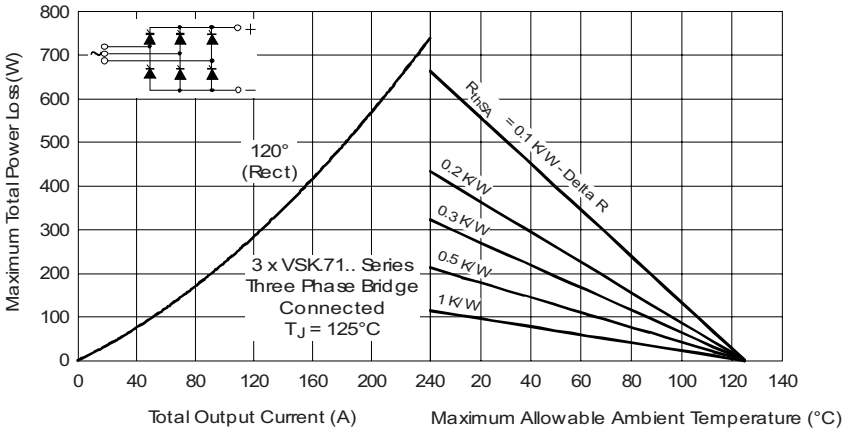


Fig. 9 - On-State Power Loss Characteristics

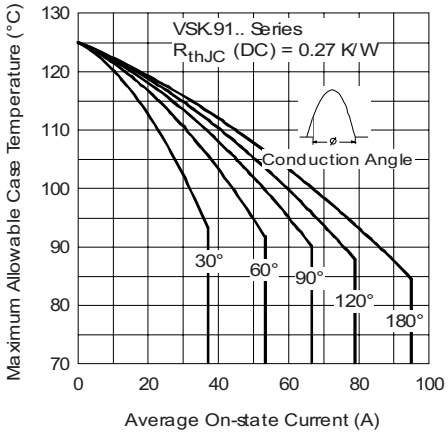


Fig. 10 - Current Ratings Characteristics

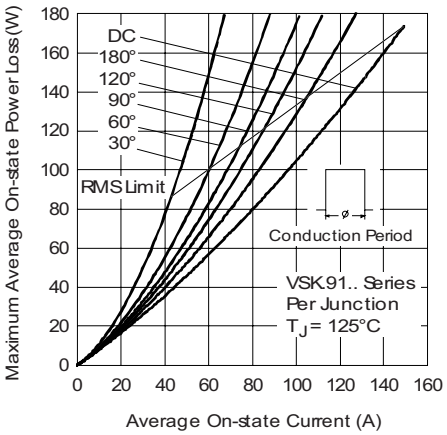


Fig. 13 - On-State Power Loss Characteristics

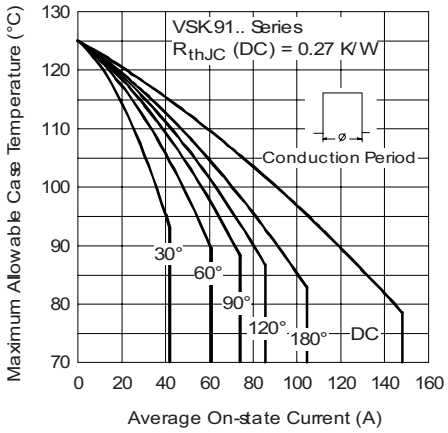


Fig. 11 - Current Ratings Characteristics

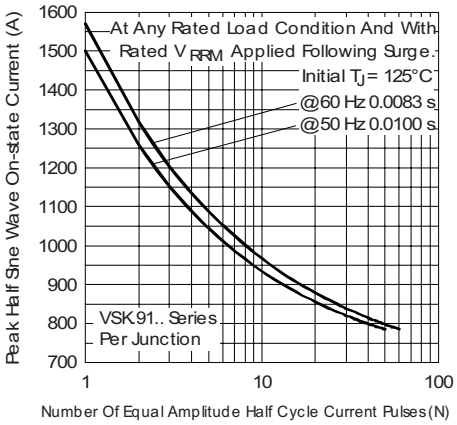


Fig. 14 - Maximum Non-Repetitive Surge Current

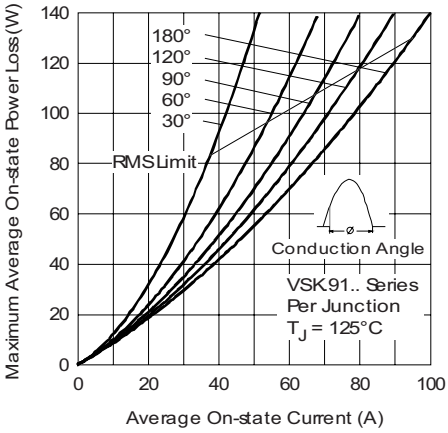


Fig. 12 - On-State Power Loss Characteristics

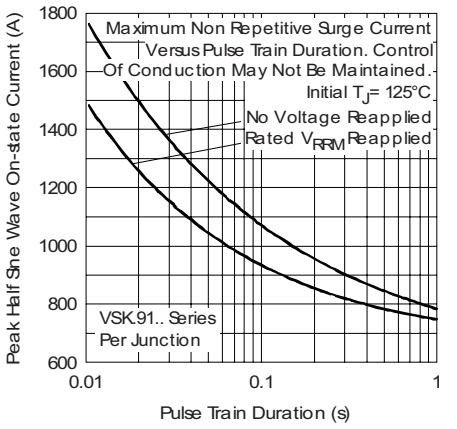


Fig. 15 - Maximum Non-Repetitive Surge Current

Thyristor/Diode and Thyristor/Thyristor
(ADD-A-PAK™ Generation 5 Power Modules),
75/95 A

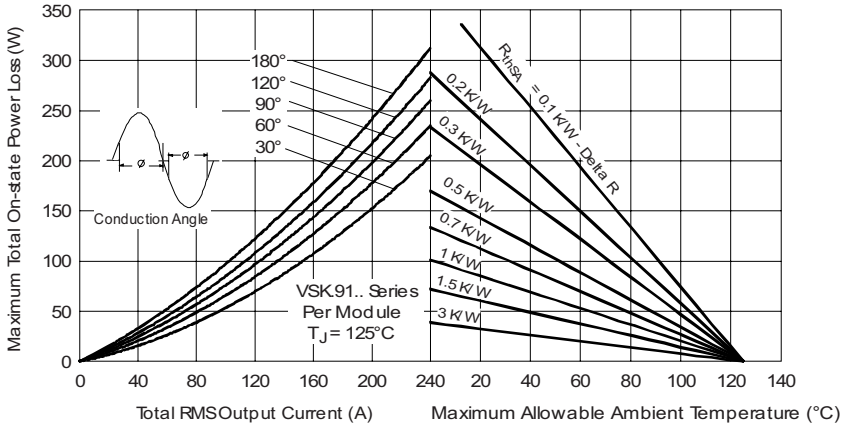


Fig. 16 - On-State Power Loss Characteristics

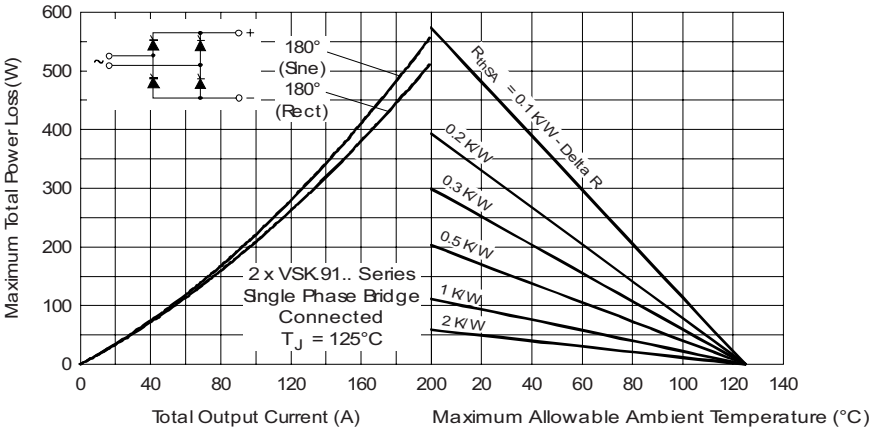


Fig. 17 - On-State Power Loss Characteristics

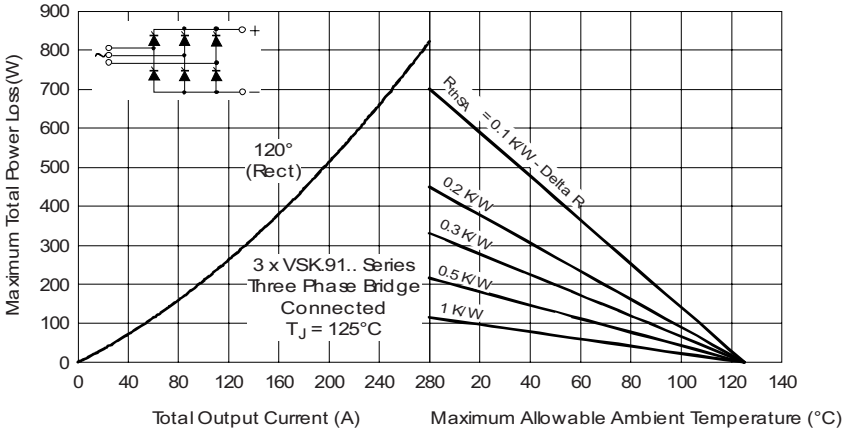


Fig. 18 - On-State Power Loss Characteristics

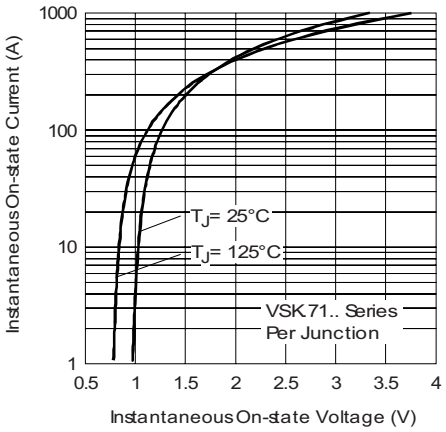


Fig. 19 - On-State Voltage Drop Characteristics

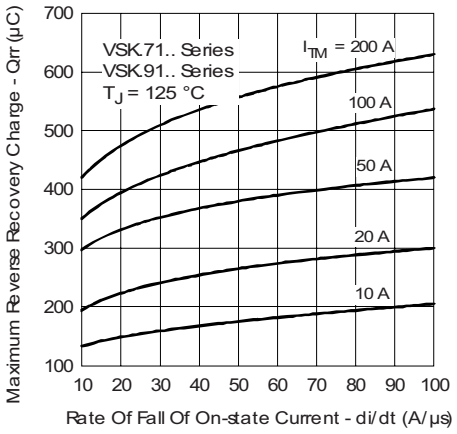


Fig. 21 - Recovery Charge Characteristics

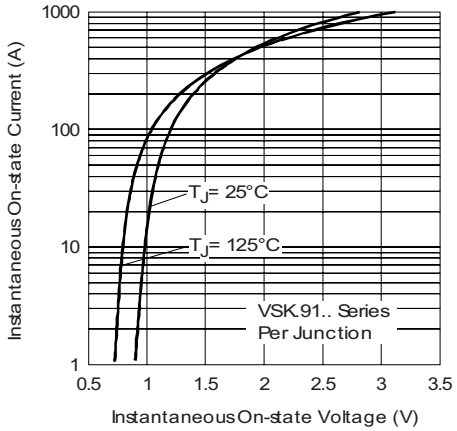


Fig. 20 - On-State Voltage Drop Characteristics

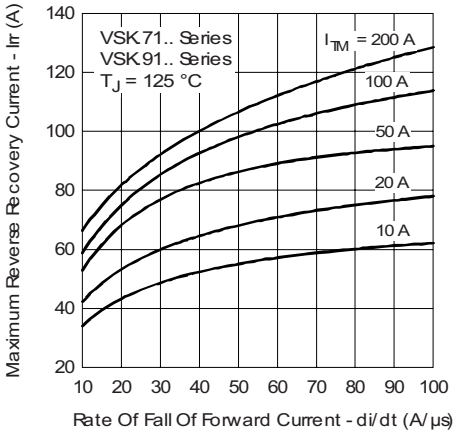


Fig. 22 - Recovery Current Characteristics

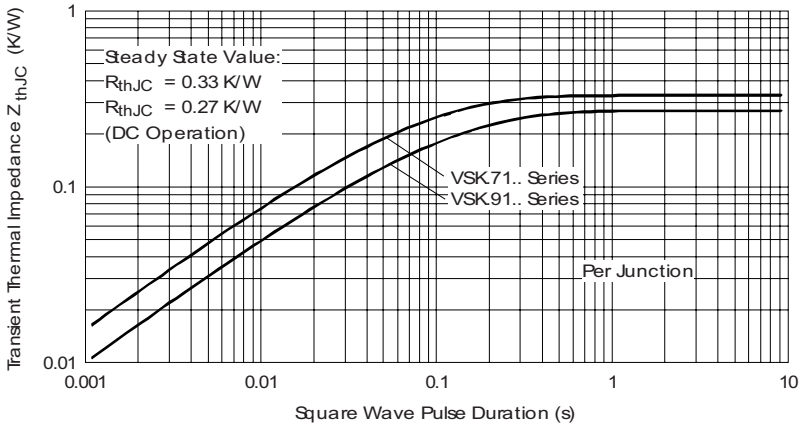


Fig. 23 - Thermal Impedance Z_{thJC} Characteristics

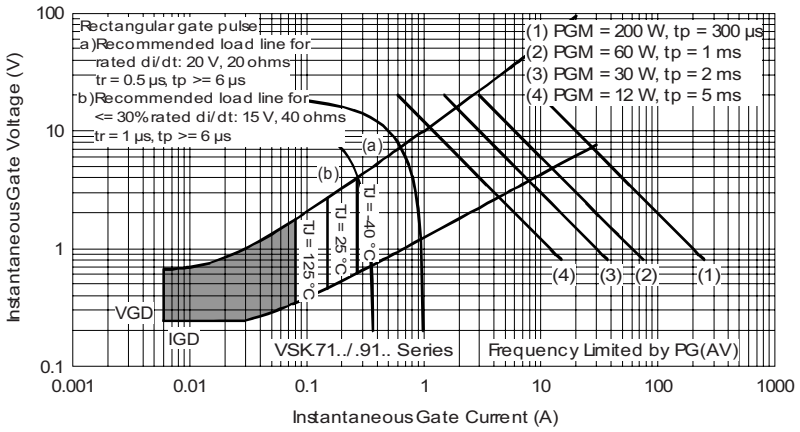


Fig. 24 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

VSK	T	91	/	16	S90	P
1	2	3		4	5	6

1 - Module type

2 - Circuit configuration (see end of datasheet)

3 - Current code (1)

4 - Voltage code (see Voltage Ratings Table)

5 - dV/dt code: S90 = dV/dt 1000 V/µs
No letter = dV/dt 500 V/µs

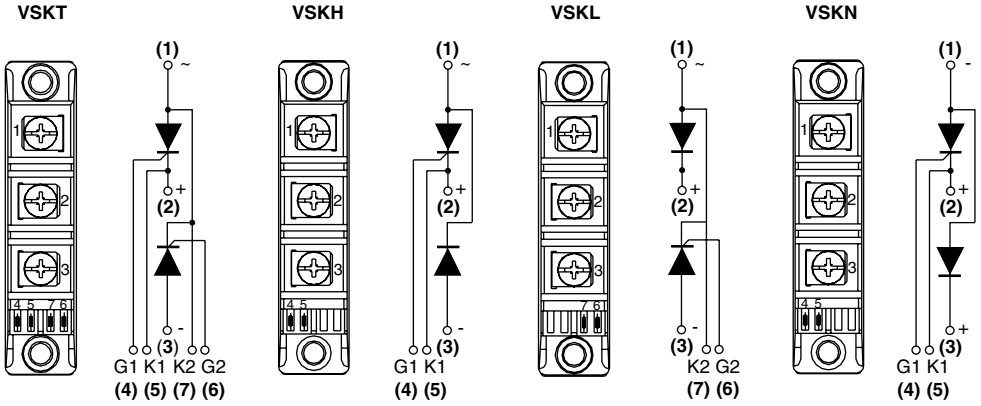
6 - P = Lead (Pb)-free

(1) Available with no auxiliary cathode
(for details see dimensions - link at the end of datasheet)
To specify change: 71 to 72
91 to 92
e.g.: VSKT92/16P etc.

Note

- To order the optional hardware go to www.vishay.com/doc?95172

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95085

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